REMARKS

Claims 1-16 and 18-30 are canceled.

Claims 17 and 31-37 are pending.

Claims 17 and 31-37 are rejected.

The final office action dated Dec. 15, 2008 indicates that base claim 31 is rejected under 35 USC §102(e) as being anticipated by Ballagh U.S. Patent No. 6,883,147. The final office action also indicates that base claim 35 is rejected under 35 USC §103(a) as being unpatentable over Ballagh in view of the admitted prior art ("APA"). These rejections are respectfully traversed.

Base claims 31 and 35 recite a CPU and FPGA for performing different portions of a numerical simulation. Base claims 31 and 35 further recite features for controlling the flow of data between the FPGA and the CPU during a numerical simulation.

These features are not taught or suggested by Ballagh. Ballagh discloses a single chip 202 that ***implements*** a processor 204, bus 206, bus-host interface 208, and peripheral component 210 (see col. 5, lines 1-11). That is, the FPGA has an embedded processor (col. 1, lines 59-64).

Ballagh does not teach or suggest two separate chips: a CPU and FPGA. Ballagh discloses a single chip 202.

Ballagh is silent about dataflow between a CPU and an FPGA. Ballagh only discloses dataflow between the embedded processor 204 and the embedded peripheral 210.

Ballagh does not teach or suggest running a first portion of a numerical simulation on a CPU and a second portion of a numerical simulation on an FPGA. Simulations of the embedded processor 204 and the embedded peripheral 210 are

performed in a computer prior to the hardware implementation in the FPGA (col. 1, lines 16-22).

Thus, base claims 31 and 35 should be allowed Ballagh.

Nevertheless, base claims 31 and 35 have been amended to further clarify these differences. Claim 31 has been amended to recite "a Field Programmable Gate Array (FPGA) and a separate central processing unit (CPU)"; and claim 35 has been amended to recite "a central processing unit (CPU) and a Field Programmable Gate Array (FPGA) for performing different portions of a numerical simulation."

The rejections over Ballagh in view of the admitted prior art are also respectfully traversed. The admitted prior art discloses the elements of a radar simulation. All elements are performed in a CPU. The admitted prior art also acknowledges a problem with the time needed to perform the simulation on a CPU (see page 2, lines 2-29 of the application). The claims recite an approach for speeding up the simulation. Ballagh does not teach or suggest the claimed approach.

An objection to the claims is respectfully traversed, since the terms CPU, FFT and FPGA are well known terms that also happen to be defined in the specification. However, since the base claims are being amended, these amendments have included the definitions. Therefore, the objection has been rendered moot.

Claim 17 has been amended to add a colon after "including" in line 2.

The Examiner is encouraged to contact the undersigned to resolve any remaining issues prior to mailing another office action.

Respectfully submitted,

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